APPLICATION NOTE

- TDA8768 -
12 BIT A/D CONVERTER
DEMONSTRATION BOARD

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- TDA8768 -
12-bit A/D CONVERTER

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SUMMARY

This **A**pplication **N**ote describes the design and the realization of the **DEMO8768** Demonstration board using a **TDA8768H** with an application environment. In order to obtain the best performances, all the main recommandations which are to be applied to design the Printed Circuit Board are also described.

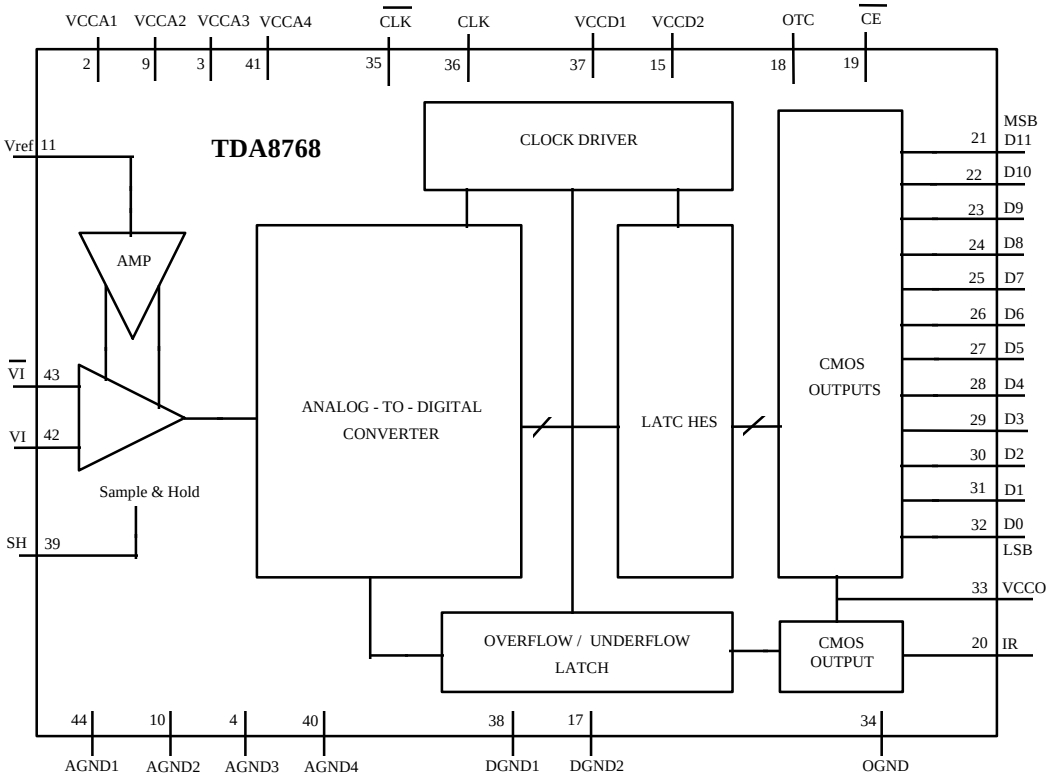
CONTENTS

1. MAIN FEATURES OF THE TDA8768H

The **TDA8768H** is a BICMOS 12-bit **A**nalog-to-**D**igital **C**onverter designed for professional applications. It can convert an Analog input signal into 12-bit binary coded digital words at a maximum sampling rate of 55 MSps with a typical power dissipation of 335 mW only. Two versions of the device exist in QFP44 package : TDA8768H/4 and /5 corresponding to the specification of the sampling rate: 40 or 55 MSps. The most frequent applications are located in the high-speed analog-to-digital conversion domains such as :

- Video signal digitizing
- Imaging (camera scanner)
- Telecommunication
- High Definition TV (HDTV)
- Medical imaging
- Base-station receiver

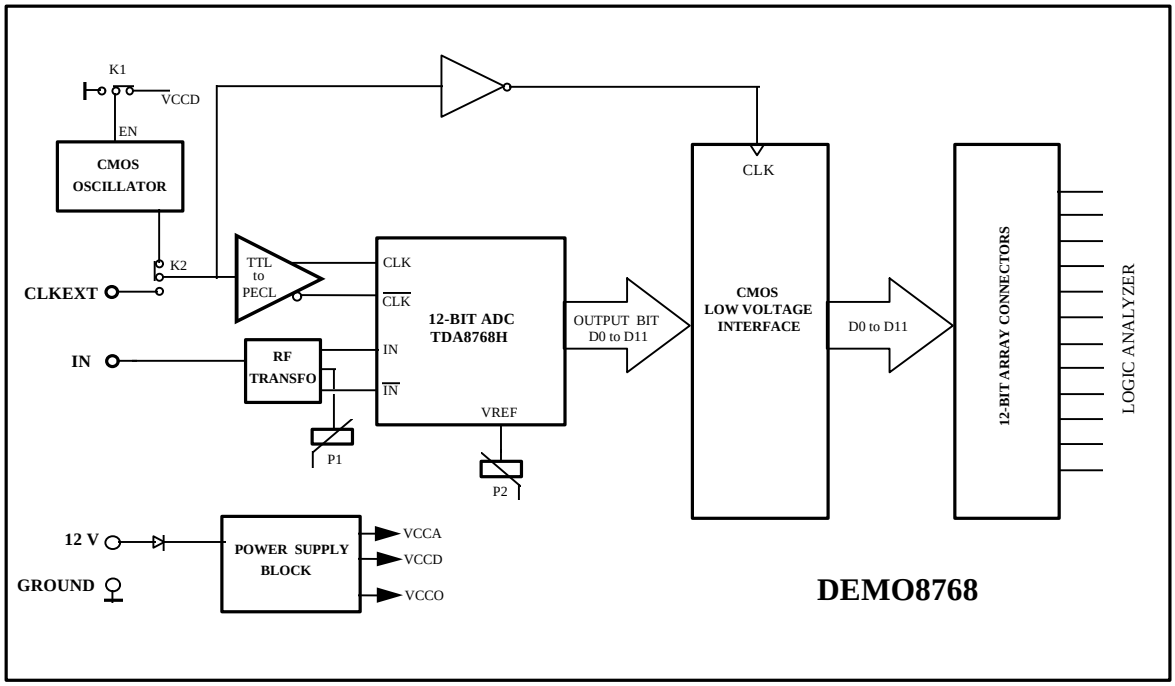
The block diagram of the device is shown on the **Figure 1** .



- FIGURE 1 -

2. PRINCIPLE AND DESCRIPTION

The principle of the Demonstration board, which is described in this Application Note, is shown on the **Figure 2**. The electrical diagram, the part list associated with the implementation scheme are given in the **"Demoboard file"** chapter of this Application Note.



- FIGURE 2 -

The different blocks constituting the board are the following :

- **A power supply block** constituted of three low power voltage regulators, to supply the VCCA, VCCD and VCCO on all circuitry on the board.

- **A three-state hybrid CMOS/TTL-Compatible clock generation circuit** to produce the internal clock signal. This circuit is associated to a **clock selector**, allowing to choose the clock operation mode of the board.

- **A 50Ω RF transformer** to transform the analog signal applied on the "IN" 50Ω SMA connector to symetrical differential mode on the analog inputs VIN and VINN of the ADC.

- **A TTL to PECL translator IC** to transform the TTL levels *(internal or external)* applied on clock selector, to PECL levels directly addressed to differential clock inputs of the ADC.

- **A TDA8768 Analog-to-Digital Converter** used to convert the analog signal applied on the "IN" 50Ω SMA connector, into 12-bit binary coded digital words *(Straight binary or 2' s complement).*

- **A Low Voltage CMOS Interface decision circuit** used to recover the ADC data output synchronized on the clock sampling falling edge. The recovered data are directly addressed on a special probe connector available on the board, to evaluate the TDA8768 in the application in the digital domain.

- **A 12-Bit array connector** to connect the probes of the logic analyzer.

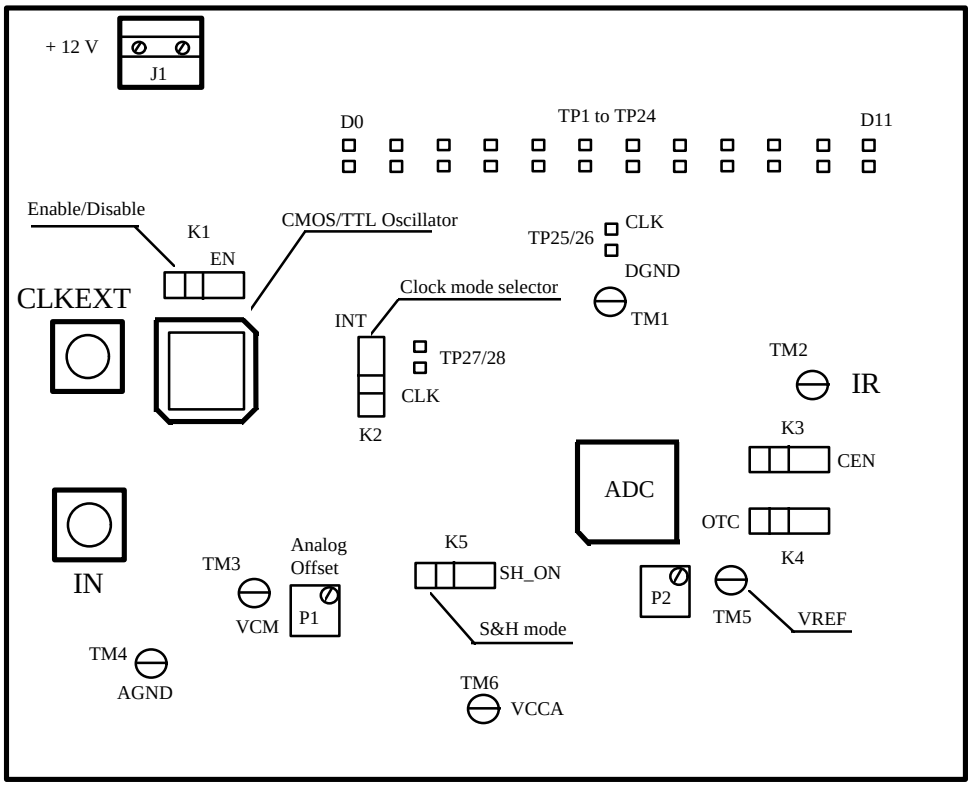
The Demonstration board is functional out of a single +12 V external power supply and all circuitry is protected from reverse polarities.

The sampling clock signal can be internal, that is to say generated on the board from a specific CMOS oscillator, or external from an 50Ω generator. The board allows to make an evaluation of the device in both clock modes, thanks to a switch and a separate clock input *(SMA connector)*. Therefore, in both cases, the clock signal of the CMOS interface circuit is derived from the ADC clock, through a specific CMOS inverter.

Before using the board, please choose your mode and refer to the corresponding "clock operating mode" chapter, to verify that the switch is correctly set.

3. OVERALL VIEW OF THE BOARD

The whole layout of this Demoboard is shown in **Figure 3**.



- FIGURE 3 -

The different connection plugs, trimmers, switches and test-points available on the board are, for :

*** General power supply**

- A connector **J1** type Phoenix to connect the demoboard to an external power supply between **+12V** and **GND**.

*** DC voltage adjustment values**

- Two chip trimmer potentiometers **P1** and **P2** to adjust respectively on the ADC from VCCA supply, the V_{CM} common mode voltage on the analog inputs and external voltage V_{REF} .

- Three control points **TM6, TM3** and **TM5** to control respectively the VCCA, V_{CM} and V_{REF} voltage values.

*** Evaluation of the TDA8768**

- One external clock input **CLKEXT** with 50Ω SMA connector **J2** *(associated to switch K2 to choose the clock mode).*

- One analog input **IN** with 50Ω SMA connector **J3** to connect the single-ended analog signal on the input of the RF transformer used to produce a symetrical differential signal applied on the ADC.

- A specific output control point **TM2** to display the In-Range data output of the ADC.

- A switck **K1** to control the chip Enable of the internal oscillator.

- Four switches **K2**, **K3**, **K4** and **K5** to command respectively the "clock mode", the "chip enable input", the "output two's complement mode", and the "sample-and-hold selection" of the ADC with the relevant CMOS levels given on the hereunder tables :

OTC	**$\overline{CE}$**	**D0 to D11 and IR**
0	0	binary; active
1	0	two's complement; active
don't care	1	high impedance

SH	**SAMPLE-AND-HOLD**
1	active
0	inactive; tracking mode

*** Reconstruction of the analog input waveform**

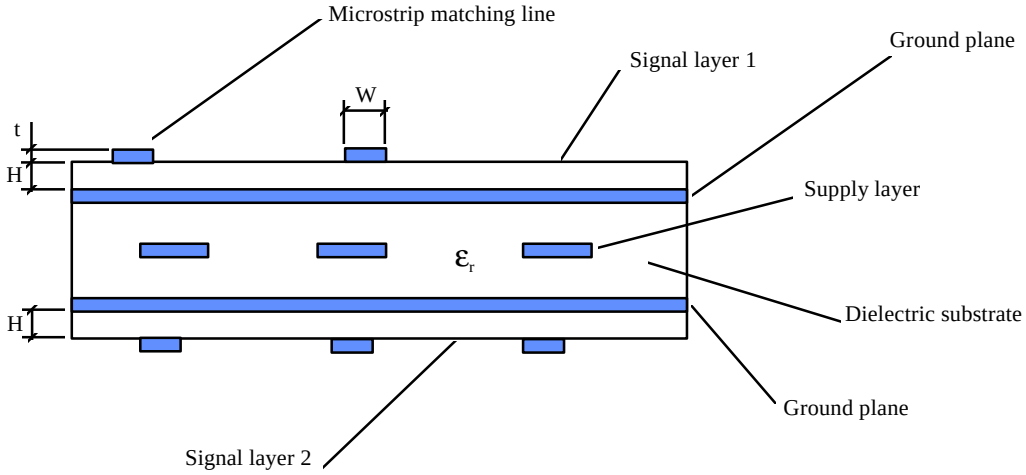
- Twelve digital CMOS-compatible outputs **D0** to **D11** with a special test points array **TP1 to TP24** to enable direct connection of the probe to the associated logic analyzer in an external data processing system.

- Two special probe test-points **TP27/28** and **TP25/26** to control respectively, the clock signal applied on the TTL to PECL translator and that obtained on the input of the CMOS interface cicuit.

- Two ground connections **TM1** and **TM4** respectively for DGND and AGND.

4. TECHNOLOGICAL CONCEPT

The practical design has been made on a multilayer **P**rinted **C**ircuit **B**oard of 3.75" x 3.45" size. The technological concept chosen to make this multilayer PCB uses five physical layers as shown **Figure 4**. The first and fifth layers are the signal layers, the second and fourth layers constitute the ground planes corresponding to signal layers. Moreover, the third layer situated between two ground planes has been provided especially to design the power wiring system.



- FIGURE 4 -

The dielectric substrate used is an Epoxy Glass resin having a relative permittivity of 4.7 and a copper thickness (t) of 35 µm. The metallized via hole technic was employed to make all necessary interconnections between layers. The global thickness of the PCB is about 64 mils (1.6 mm) with a thickness (H) between signal layers of 8 mils (0.2 mm).

4.1 MICROSTRIP LINE COMPUTATION

So, all the 50Ω matched lines were designed with the microstrip technology and the width (W= 12.7 mils) of these lines determined from the following Kaup's relation :

$$W = \frac{7.475H}{exp\left(Z_C\sqrt{e_r + 1.41}\,/\,87\right)} - \frac{t}{0.8}$$

4.2 DIGITAL AND ANALOG GROUND REQUIREMENT

In order to minimize the noise due to capacitive coupling between the digital and analog input parts of the ADC, two separated ground planes were designed on all layers of the Demo-Board. The digital and analog power supplies were returned to a single ground-point located under the device.

4.3 SUPPLY WIRING LAYOUT

To prevent it from stopping the ground planes of the line technological structure, the supply wiring system of all circuitry on the demo-board has been made on the internal third layer.

Moreover, in order to reduce the voltage fluctuation effects due to switching currents inside the different IC devices, the DC supply currents are driven to the devices by very low characteristic impedance microstrip lines having a small equivalent inductance. The lengths of all these supply lines were designed in order to limit the voltage drop value to lower than one percent of the power supply value.

4.4 EMC - REQUIREMENT

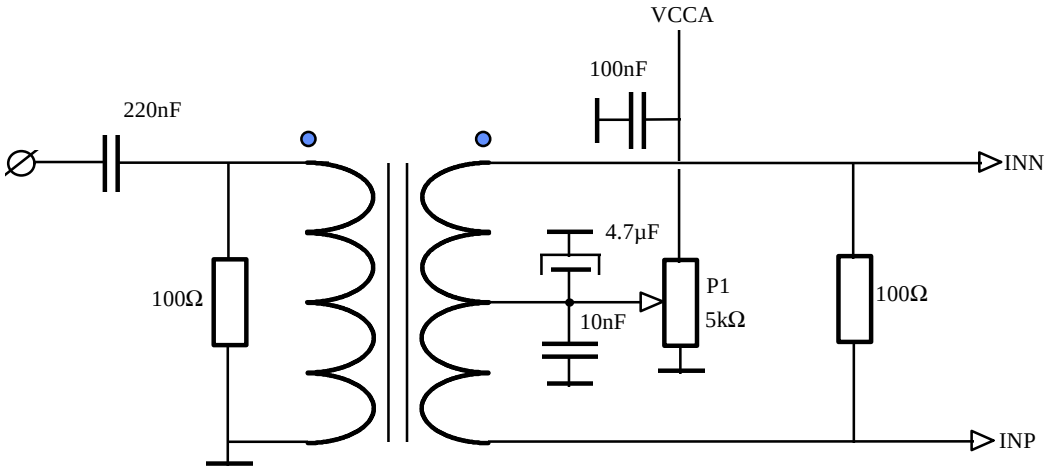
In order to satisfy the **E**lectro-**M**agnetic **C**ompatibility requirements and to ensure a good Power Supply Rejection Ratio on the different supply pins and to suppress an eventual close-in coverage risk, each supply line close to ADC is wideband bypassed *(see Chapter 5 § 4).*

5. SPECIAL FEATURES OF THE TDA8768

In order to obtain the optimal performances, the advised Application scheme of the TDA8768 is shown on the **Figure 21** on the "Demoboard file" chapter. However, several requirements must be satisfied about the following specific points described in this chapter.

5.1 ADC ANALOG INPUT

A wideband RF transformer is used to make the adaptation between the Analog input of the board and the differential analog inputs of the ADC as shown on the **Figure 5**.



- FIGURE 5 -

The DC common mode voltage is fixed on the middle point of the transformer secondary, by the trimming potentiometer P1 which allows, from the VCCA supply voltage, to adjust, on the board, the common mode voltage at the specified value V_{CM} = 3.6V. Moreover, to ensure a sufficient analog input stability, the current I_P in P1 was fixed at about 1mA taking into account the specified high *(or low)* level analog input current *(10 µA)* of the ADC. A wideband frequencies decoupling of 4.7µF in parallel with 10nF has been added on the middle point of the transformer secondary, to get a good "dynamic" ground.

The dynamic analog signal is connected through a 220nF AC coupling to the input RF transformer via a 50Ω microstrip matched line and a SMA plug-in connector. So, the symetrical and differential analog signal is applied on the analog inputs INN and INP of the ADC. The secondary load of the RF transformer was fixed to 100Ω in order to ensure a 50Ω matching with regard to an **analog virtual ground.** In this condition, with a transformer ratio of n=1 the primary brought back impedance is 100Ω. Consequently, the 50Ω impedance matching to the external generator is performed with a resistor of 100Ω in parallel on the primary of the transformer.

The differential Full-Scale voltage V_{FS} which can be applied on the differential analog inputs of the ADC is dependent of the differential DC voltage *(VCCA - V_{REF})* whose the specified V_{REF} value *(with the condition VCCA=5V)* is :

$$V_{REF} = 3.175\ V$$

So, with this condition, the guaranted Full-Scale analog input value applied on the pin device is :

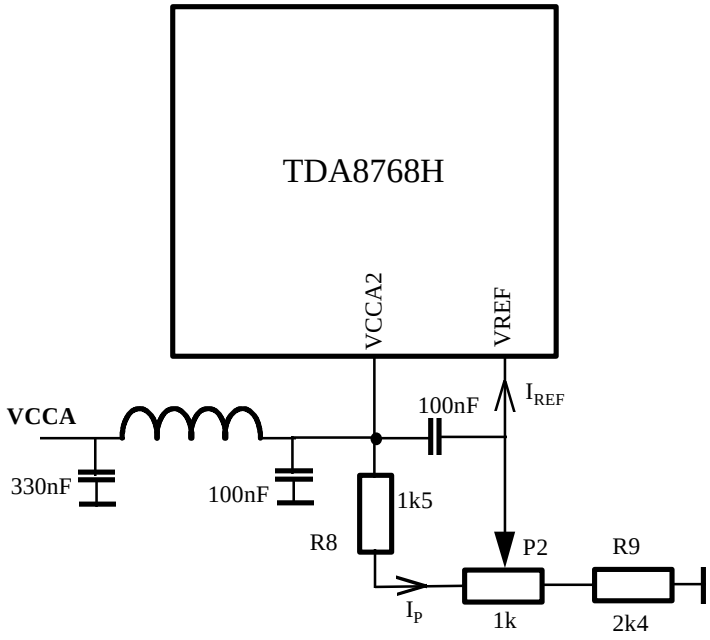
$$| V_{INP} - V_{INN} |_{(p.-p)} = V_{FS} = 2.0\ V$$

Consequently, for 2^{12} codes of the analog input signal, the typical value of the Least Significant Bit *(LSB)* is :

$$LSB = \frac{V_{FS}}{2^{12} - 1} \qquad \text{so,} \qquad LSB \approx 488.4\ \mu V.$$

5.2 REFERENCE VOLTAGES VREF

The Reference voltage of the ADC is adjusted on the device pin V_{REF} with a trimming potentiometer P2 associated to the resistor bridge R8 and R9, as shown on the **Figure 6**.



- FIGURE 6 -

As the Full-Scale voltage is dependent on the VCCA and V_{REF}, these two voltage values must be very stable. Consequently, a precision regulator will be used to obtain the VCCA voltage value *(see "VCCA voltage regulator" paragraph inclosed in the following chapter)* and in order to ensure a sufficient stability on the V_{REF} voltage the current I_P in the resistor bridge will must to respect the condition $I_p \geq 20\ I_{REF}$. Moreover, in order to ensure a distribution of the noise level obtained on VCCA, the V_{REF} device pin must be bypassed and referenced to VCCA supply pin. In fact, with the simple configuration, and taking into account :

- of the thermal coefficient of 150ppm/°K of the VCCA precision regulator output voltage,

- of the thermal coefficients of 250ppm/°K and 100ppm/°K respectively for the bridge resistor R8/R9 and the trimming potentiometer P2,

the maximum drift coefficient of the differential DC voltage (VCCA - V_{REF}) is :

$$\Delta\ (VCCA - V_{REF}) \pounds\ 0.3\ mV/°K$$

5.3 DATA OUTPUTS DO TO D11

On the Demonstration-Board each data output is directly addressed to the corresponding input of the CMOS interface circuit. The typical values, referenced to AGND, of the coding and ADC analog input voltage are given in the hereunder table :

STEP	V_{INP}	V_{INN}	IR	BINARY OUTPUTS D11 to D0	TWO'S COMPLEMENT OUTPUTS D11 to D0
underflow	< 3.1	>4.1	0	000000000000	100000000000
0	3.1	4.1	1	000000000000	100000000000
1	-	-	1	000000000001	100000000001
↓	-	-	↓	↓	↓
2047	3.6	3.6	1	011111111111	111111111111
↓	-	-	↓	↓	↓
4094	-	-	1	111111111110	011111111110
4095	4.1	3.1	1	111111111111	011111111111
overflow	>4.1	< 3.1	0	111111111111	011111111111

All data outputs D0 to D11 of the TDA8768 are obtained through compatible CMOS buffers inside the device which are supplied with 3 Volts from VCCO power supply. The guaranteed logic levels with a maximum capacitive load *(per bit)* C_L = 10pF are the following :

$$V_{OL}\ max = 0.5\ V \qquad V_{OH}\ min = VCCO - 0.5\ V$$

In the above conditions the typical output transients t_T *(10 to 90%)* under VCCO = 3 Volts is :

$$t_T = 4.0\ ns$$

Consequently, an estimation of the output slew-rate *(dV/dt in V/ns)* and of the bit switching current *(I_0 in mA/bit)* can be made from the hereunder relations :

$$\frac{dV}{dt} = \frac{80\%\left(V_{OH} - V_{OL}\right)}{t_T} \qquad I_0 = C_L \frac{dV}{dt}$$

hence, $dV/dt = 0.6\ V/ns$ and $I_0 = 6\ mA/bit$

Consequently, the Full-Scale transition output switching current $I_{0FS} = N.I_0$ *(where N is the number of bits of the ADC)* is :

$$I_{0FS} = 72\ mA$$

Note : In the application where the 5 V Output power supply VCCO is used, the output transient value is reduced at 2.5ns. Consequently, the output switching current per bit and Full Scale are respectively :

$I_0 = 16\ mA/bit$ and $I_{0FS} = 192\ mA.$

The output buffers of the TDA8768 were designed to support these values of the output switching current. But, for certain applications where the capacitive bit load is higher than 10pF, a limiting serial resistor may be necessary to adapt the slew-rate value without risk with regard to ADC output buffers.

Moreover, in order to reduce the delay between data, each line must be of the same length. This length was determined taking into account the following values :

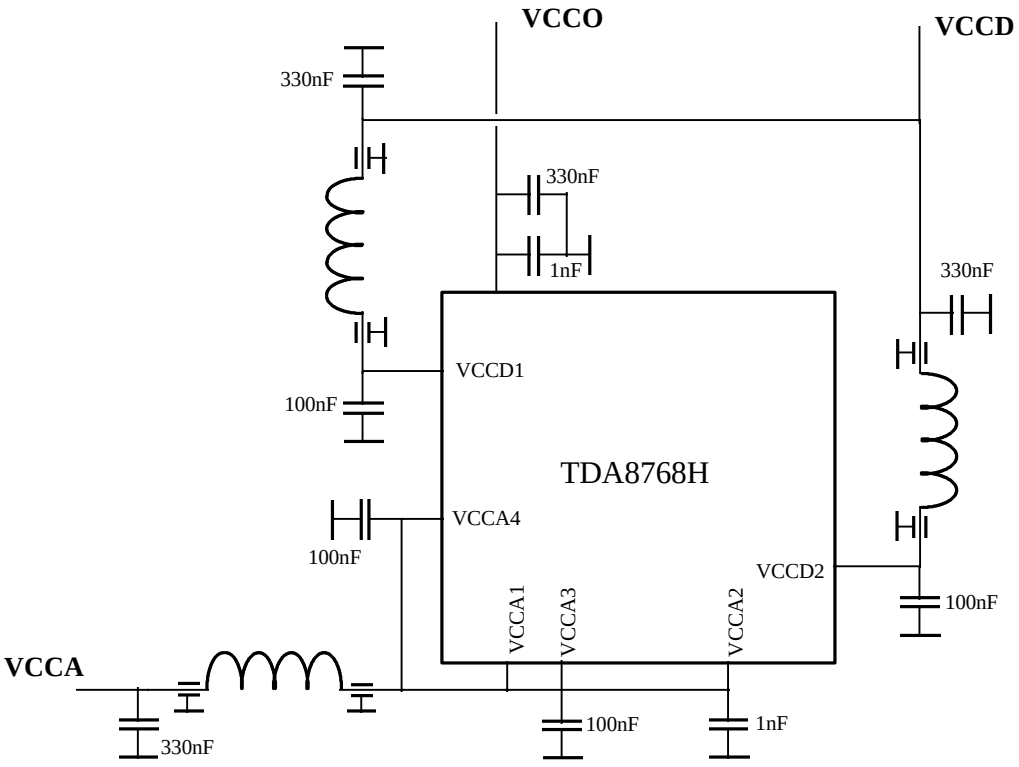
- The specified maximum output capacitance load : C_L = 10 pF.
- The maximum input capacitance of the CMOS interface *(On Demo- Board)* : C_{IN} = 5.0 pF.
- The distributed capacitance on the line : C_0 = 1.13 pF/cm.

In order to satisfy :

$$L_D \le \frac{C_L - C_{IN}}{C_0} \qquad \text{so} \qquad L_D \pounds\ 4.4\ cm$$

5.4 ADC ANALOG AND DIGITAL POWER SUPPLIES

In order to obtain a good dynamic rejection on the ADC supply pins, the Analog VCCA and Digital VCCD supply lines are addressed to the supply pins of the ADC through three SMD bypass pi filters as shown by the schematic supply diagram of the **Figure 7**.



- FIGURE 7 -

These bypass pi filters were implanted near the ADC to separate each power supply of the device, the VCCO supply line is directly addressed to the specific pin of the ADC output digital part. Moreover, the PCB layout has been designed so that the power supply line end arrives close to the VCCA, VCCD and VCCO sides. These points are perfectly decoupled with 330nF and 100nF ceramic capacitors close to respective supply pin of the device.

Note : Therefore, if one +5V power supply only is used, it is advised also to use a bypass pi filter to separate each power pins VCCA and VCCD and to obtain a good dynamic rejection of the clock signal on the supply lines. In this case the PCB layout must be designed in order that the general power line end arrives directly close to the VCCO side perfectly decoupled.

5.5 ADC CLOCK INPUT

The TDA8768 can work with Logic Standard PECL or with the minimum condition AC driving mode as mentionned in the following table :

MODE	CLKP	CLKN
PECL	PECL	3.65 V *(DC)*
	3.65 V *(DC)*	PECL
	PECL	PECL
AC	0.5 Vp.-p	2.5 to 3.65 V *(DC)*
	2.5 to 3.65 V*(DC)*	0.5 Vp.-p
	0.25 Vp.-p	0.25 Vp.-p

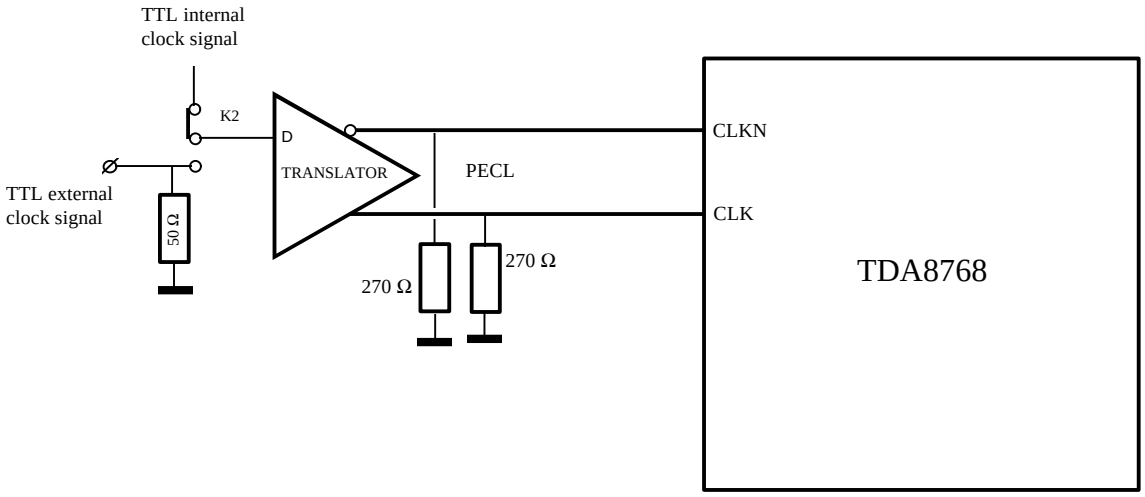
The required PECL limit levels and AC amplitude on the clock pins of the device are the following :

MODE	V_{IL}	V_{IH}
PECL	3.52 V	3.83 V
AC	0.5 Vp.-p	

In order to improve the transient on the clock signal and to obtain a maximum speed and the best control between the clock and output transition as well as minimal noise, the clock input signal is applied in differential mode on the CLKP and CLKN pins of the device.

On the **Demonstration-Board** the clock signal *(external or internal)* is conform to TTL standard Logic levels.

A special TTL to PECL translator circuit is used to make the adaptation between the TTL external *(or internal)* clock input applied on the switch mode selector K2 and the PECL differential clock input of the ADC as shown on the **Figure 8**.



- FIGURE 8 -

On the Demonstration-Board, the PECL clock signal is driven through 50Ω microstrip lines shorted on the ADC differential clock inputs. In fact, in order to limit the reflection on the clock signal, the length of the clock lines must be lower than one inch.

The emitter-follower output stages of the translator IC were loaded by 270Ω referenced to digital ground. Consequently, with this configuration, the PECL output impedance is low *(about 7W)* and the PECL average DC level applied on the clock inputs is about 3.6 V.

The clock jitter must be sufficiently low in order to avoid the sampling errors which can appear. Consequently, the clock jitter requirement value can be determined from the slope of the analog input signal. In fact, if the equation of the sinewave analog input signal is :

$$S(t) = \frac{A}{2} sin(2p.Ft)$$

with,
- $A = 2^N$ LSB : the ADC full-scale amplitude
- N : the bit number *(resolution)* of the ADC
- F : the analog input sinewave frequency.

The slope of this signal is given by :

$$\frac{dS(t)}{dt} = \frac{A}{2} 2p.F\cos(2p.Ft)$$

with the slope maximum value when t=0 *(input voltage level is around middle code 2047/48).*

$$\frac{dS(0)}{dt} = Ap.F = 2^N LSBp.F \qquad (V.s^{-1})$$

The following approximation :

$$dt = t_{LSB}$$

corresponding to the time where the middle code is available on the ADC input, allows to write :

$$\frac{LSB}{t_{LSB}} = 2^N LSBp.F$$

after reduction we obtain the authorized referent clock jitter value :

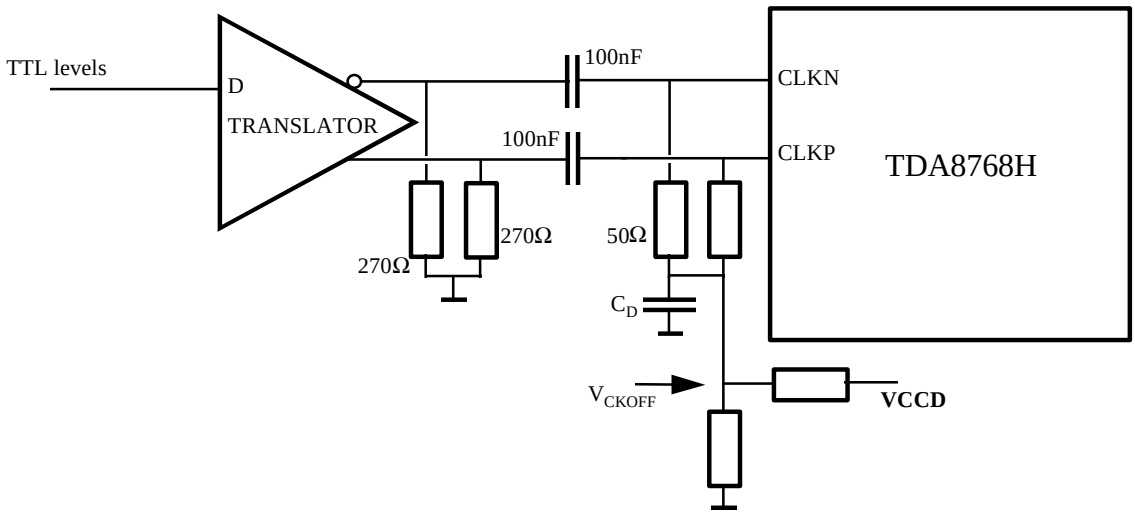
$$t_{jitt} = t_{LSB} = \frac{1}{2^N p.F}$$

So, the authorized maximum clock jitter is inversely proportional to analog input frequency. Thereby, the hereunder table gives the computed values according to different analog input frequencies :

F (MHz)	$\mathbf{t}_{jitt}$ (ps)
1	77.7
5	15.5
10	7.8
15	5.2
20	3.9
25	3.1

Note that, if the clock frequency and the input signal frequency have the same jitter (or phase noise), the sampling error due to jitter can be avoided.

Note 1: An other possibility can be offered to drive the differential clock signal from a TTL to PECL translator gate as shown on the **Figure 9**.



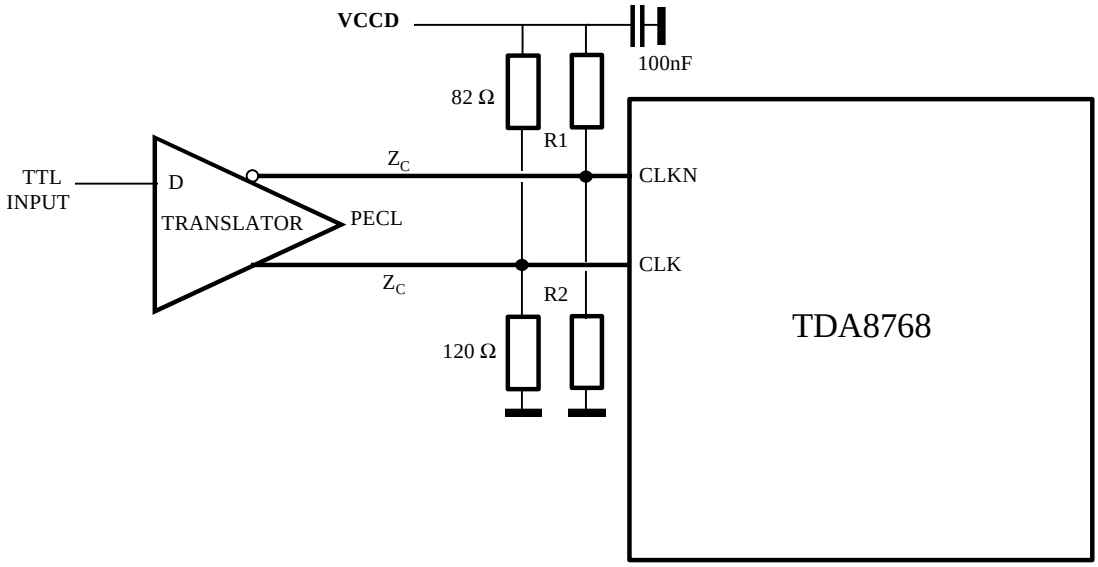
- FIGURE 9 -

The differential clock signal, *(from PECL circuit output)* is AC coupled to the clock inputs of the ADC through 100nF capacitors and 50Ω matched lines. These are shorted by 50Ω resistors referenced to offset voltage V_{CKOFF} *(between 2.5 and 3.65 V)*, near clock pins of the device. The decoupling capacitor C_D ensures a good dynamic ground of the reference point.

A specific resistor bridge ensure the clock offset voltage with a bridge current I_P which must respect the condition : $I_P \geq 20\ I_{IH/L}$ *(the absorbed current in the clock input).*

With the PECL normal working conditions corresponding to the above diagram, the peak to peak amplitude of the clock signal applied on the differential clock inputs of the ADC is higher than 0.5 Vp.-p.

Note 2 : The clock inputs of the TDA8768 can be also driven in differential from a TTL to PECL translator using the Thevenin parallel termination method, as shown on the diagram of the **Figure 10**.



- FIGURE 10 -

This method allows to obtain a reference voltage V_{TT} = 3 V *(currently used in standard PECL logic family)* on the dynamic load and to ensure the matching of the clock transmission lines. The value of R1 and R2 must be chosen in order to satisfy the following relations :

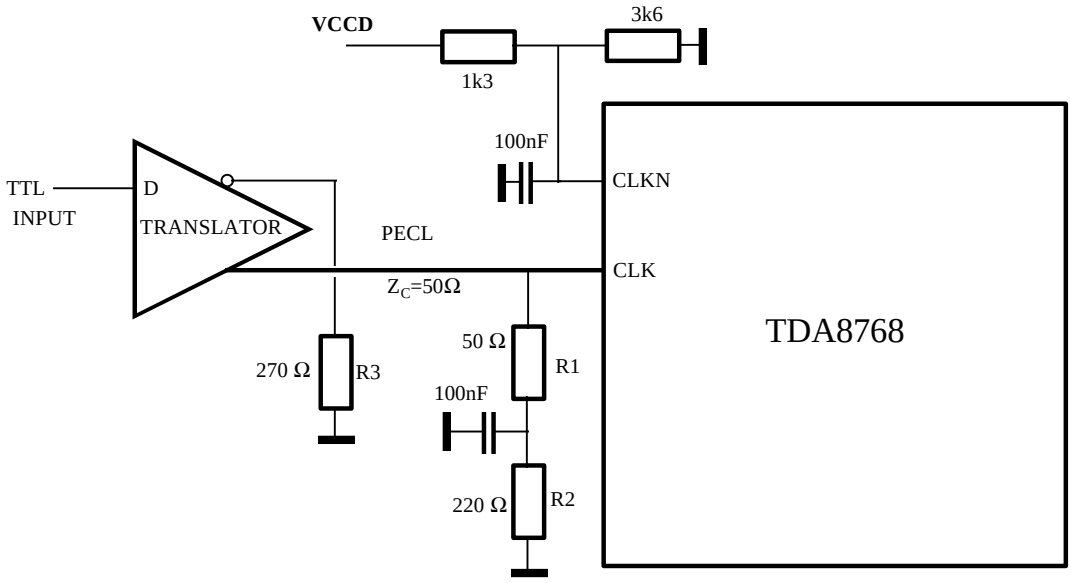
$$V_{TT} = VCCD \cdot \frac{R2}{R1 + R2} \qquad \text{and} \qquad Z_C = \frac{R1 \cdot R2}{R1 + R2}$$

for V_{TT} = 3 V, the output termination voltage reference for open emitter follower outputs and Z_C = 50 Ω, the characteristic impedance of the transmission line, we can choose after computation :

$$R1 = 82\ W \qquad \text{and} \qquad R2 = 120\ W$$

Moreover, in order to reduce the reflection freak the resistor bridges must be located near the clock pins of the ADC.

Note 3 : The clock inputs of the TDA8768 can be also driven in single-ended from a TTL to PECL translator in using the dynamic 50Ω parallel termination method, as shown on the diagram of the **Figure 11**.



- FIGURE 11 -

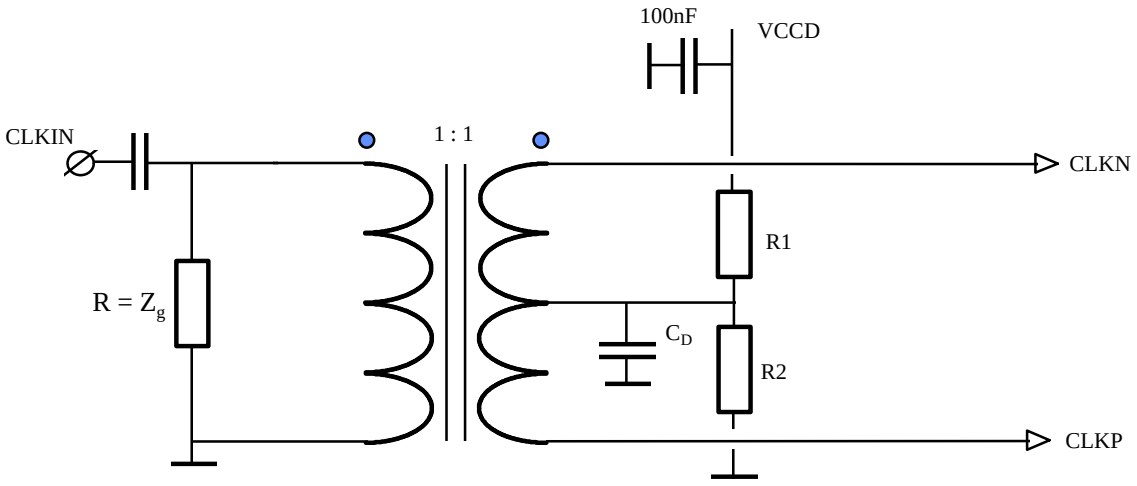
In this configuration, the 50Ω dynamic PECL load is directly referenced to DC voltage *(V_{TT} =3V)* obtained on the middle point of the resistor bridge R1/R2, a capacitor of 100nF ensure a good "dynamic ground" of this point.

With a PECL switching reference voltage V_{BB} = 3.65V specified from the PECL output levels *(V_{BB} = [V_{OH}+V_{OL}] /2)* and a characteristic impedance of the transmission line of Z_C = 50Ω *(corresponding to the R1 value)*, the R2 value is obtained from the following relation :

$$R2 = \frac{V_{TT} \cdot Z_C}{V_{BB} - V_{TT}}$$

after computation we can choose R2 = 220Ω and R3 = 270Ω *(correspondig to R1+R2)* in order to ensure the static balancing voltage on the differential output stage of the PECL translator. Moreover, the DC offset voltage V_{CKOFF} = 3.65V on the clock input CLKN can be created with a resistor bridge and a bridge current much higher than the high clock input current. A capacitor of 100nF ensures the decoupling of the DC offset voltage point.

Note 4 : The clock inputs of the TDA8768 can be easily adaptable to all Logic Families or AC coupling with the use of the specific wideband RF transformer as shown on **Figure 12**.



- FIGURE 12 -

In this condition, the matching RF transformer has a 1:1 impedance ratio and the primary load resistor R must be chosen to match the source impedance Zg, *(the high input impedance of the TDA8768 is without effect in most of the cases).* The supplied peak to peak amplitude delivered by the source signal must be higher than 500 mVp.-p.

The DC offset voltage *(between 2.5 to 3.65V)* on clock inputs is fixed, on the middle point of the transformer secondary with the resistor bridge R1/R2. To ensure a sufficient stability of the DC offset, the biasing current in resistor bridge much higher than the specified high level input clock current I_{IH} *(400µA).*

The dynamic ground is ensured on the secondary middle point of the transformer with a wideband decoupling C_D *(an association with 4.7µF in parallel with 100nF can be sufficient).*

5.6 SAMPLE & HOLD FUNCTION

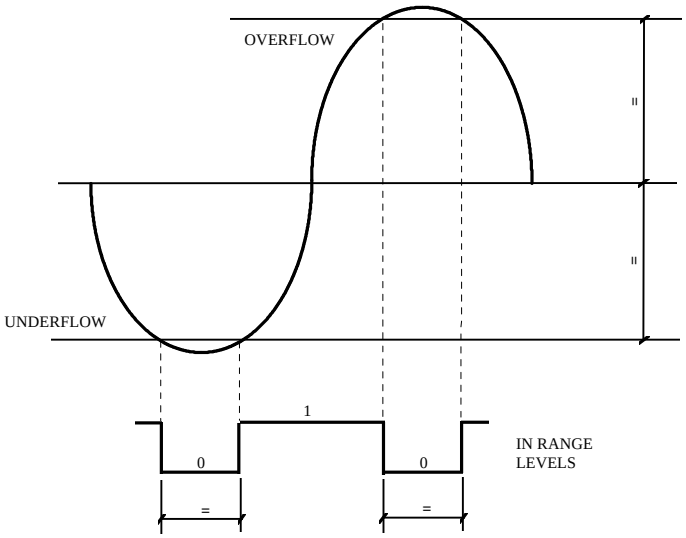
In order to ensure a digital conversion of a wideband analog signal with a high sampling rate, a Sample & Hold *(S & H)* circuit was designed inside the TDA8768. The activation of this S&H can be made with a TTL logic high level applied on the device pin SH. The levels directly available on the Demo-Board from a specific switch, are the following :

S & H FUNCTION	COMMAND LEVEL
ON	VCCD
OFF	DGND

The choice of the activation of the S&H is directly depending on the clock frequency value. The internal memory capacitor value of the S&H is sufficiently low to ensure a good efficiency of this one, above a 2 MSps of sampling rate. Below, it is better to disable the S/H function.

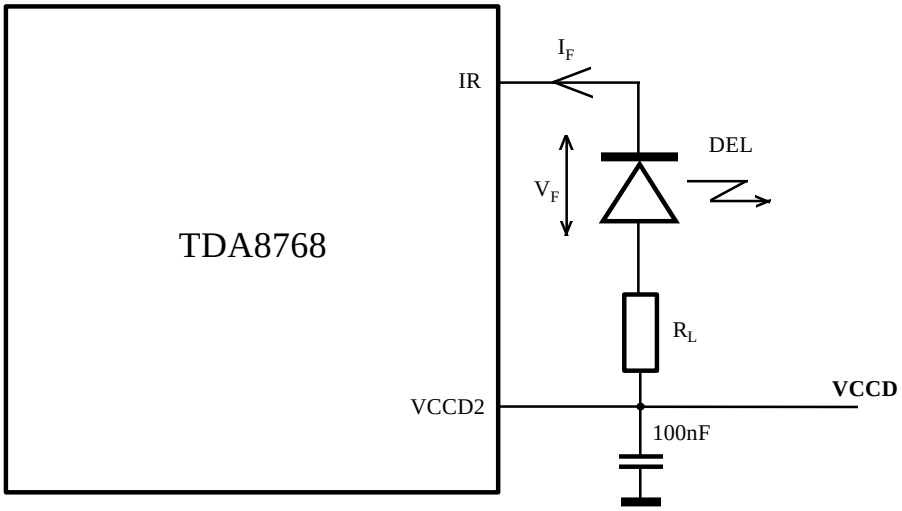
5.7 IN RANGE CONTROL

The **In-Range** output *(active high)* is available on the Demo-Board on a special measurement point. As shown **Figure 13** the under/overflow and centering of the analog signal can be controlled with the CMOS output low level duration.



- FIGURE 13 -

Note : The overange can be displayed with a Low current **L**ight-**E**lectro **D**iode, as shown on the diagram of the **Figure 14**.



- FIGURE 14 -

The limitig resistor R_L can be evaluated from the following relation :

$$R_L = \frac{VCCD - V_F - V_{OL}}{I_F}$$

with :

VCCD : the digital power supply *(5 V)*

V_F : the Forward voltage of the LED *(about 1.8 V typ.)*

I_F : the Forward current in the LED *(about 2 mA)*

V_{OL} : the IR output low level *(0 V).*

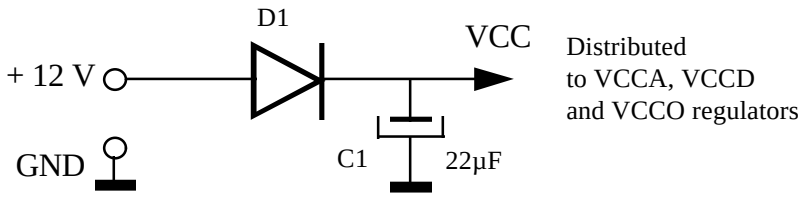
Taking into account of these values a limiting resistor value R_L*=1 kW* is sufficient.

6. ENVIRONMENT CIRCUITS

This chapter describes all circuitry diagrams implanted on the Demo-Board, but these ones are not restrictive, other circuits can also be studied according to the applications and wished performances

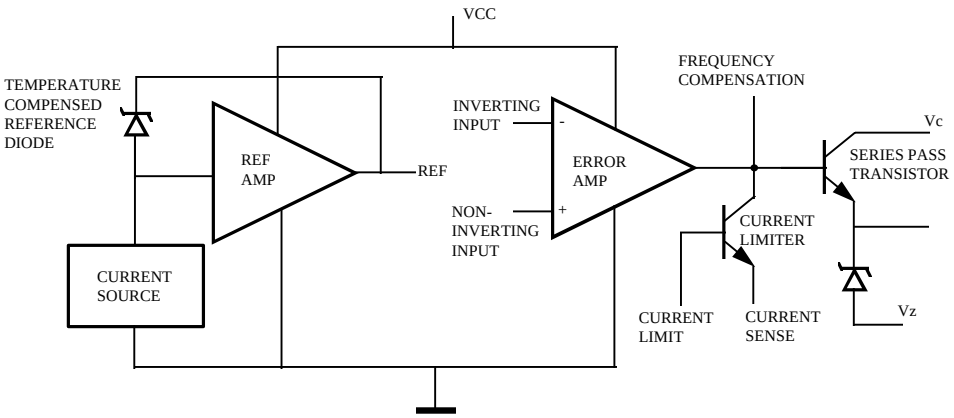
6.1 GENERAL POWER SUPPLY

As shown hereunder this circuit allows to obtain the voltage VCC necessary to supply the VCCA, VCCD and VCCO specific regulators from an external power unit of 12V/0.5A, *(the external voltage can be comprised between 10 and 15 Volts).* The SMD type BYD17G Silicium diode D1 ensures the protection of all the circuitry from reverse polarities and C1 a low frequencies decoupling made before the supply line network distributed to specific regulators. Under the external power supply nominal value + 12 Volts, the consumption is lower than 200mA.



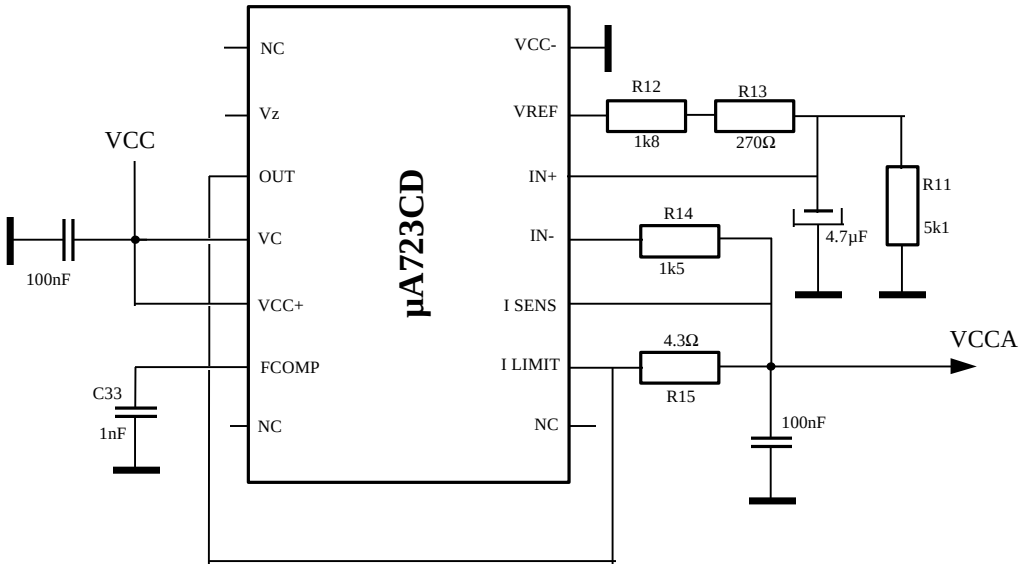
6.2 ANALOG VOLTAGE REGULATION - VCCA

The precision voltage regulator IC type µA723CD of PHILIPS SEMICONDUCTORS, whose functional block diagram is shown **Figure 15**, was used and mounted as a positive low-voltage regulator.



- FIGURE 15 -

The proposed circuit is shown in the **Figure 16**. The voltage level VCC obtained on the cathode of the protection diode D1, is applied on the VCC+ *(pin 12)* of the device. The nominal VCCA level of 5.0 V is obtained from the voltage level supplied by the VREF *(pin 6)* of the µA723CD. A resistor bridge R11, R12 and R13 allows to obtain the VCCA level value on the non-inverting input IN+ *(pin 5)* of the IC. Thereby, the dynamic balance of the integrated error amplifier is made with R14 connected between the inverting input IN- *(pin 4)* and the VCCA output voltage point.



- FIGURE 16 -

Moreover, to obtain a good output stability, the value of R14 must be equivalent to the dynamic value of the reference resistor bridge. Consequently, taking into account R11, R12 and R13 values we have chosen a resistor value of 1.5kΩ.

The output current limiting is ensured from the start conduction of the internal IC limiter current transistor with a VBE voltage level of 0.65V. So, the resistor R15 connected between I LIMIT *(pin 2)* of the IC and the regulated point VCCA output, allows to control the output limiting current ICCA. With R15 = 4.3Ω the limiting current value ICCA is obtained from the relation :

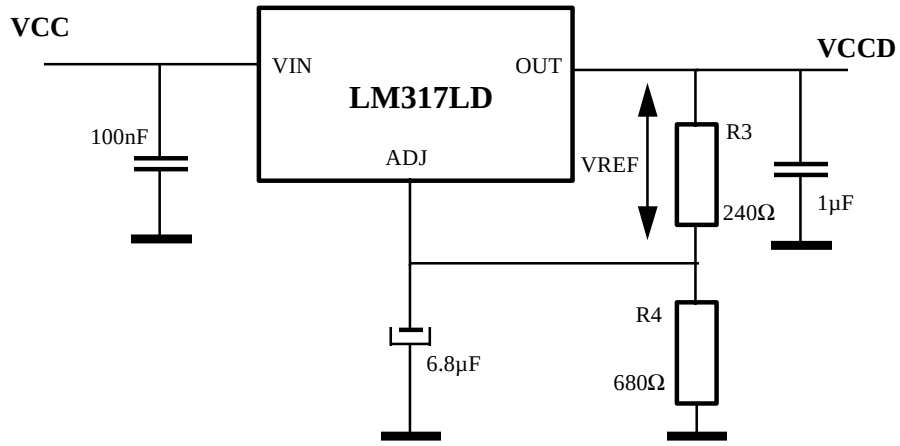
$$ICCA = \frac{0.65}{R15} \qquad \text{thus,} \qquad ICCA \approx 150\ mA$$

This maximum value is quite sufficient to drive the current into the offset resistor bridge of the analog input, VCCA supply and the VREF control loop of the ADC.

The frequency compensation of the output current amplifier stage is done with an external capacitor C33 = 1 nF .

6.3 DIGITAL VOLTAGE REGULATION - VCCD

The proposed electrical diagram is shown on the **Figure 17**. This circuit uses a low current adjustable voltage regulator type LM317LD of SGS-Thomson in SMD package SO8. This one allows to obtain the VCCD regulated voltage of 5V from VCC input voltage, and to supply a maximum output current of 100mA.



- FIGURE 17 -

From the internal reference voltage V_{REF} = 1.25V of the regulator IC, the VCCD output voltage is obtained from the relation :

$$VCCD = V_{REF} \cdot \frac{R4 + R3}{R3}$$

with R3 = 240Ω fixed we obtain :

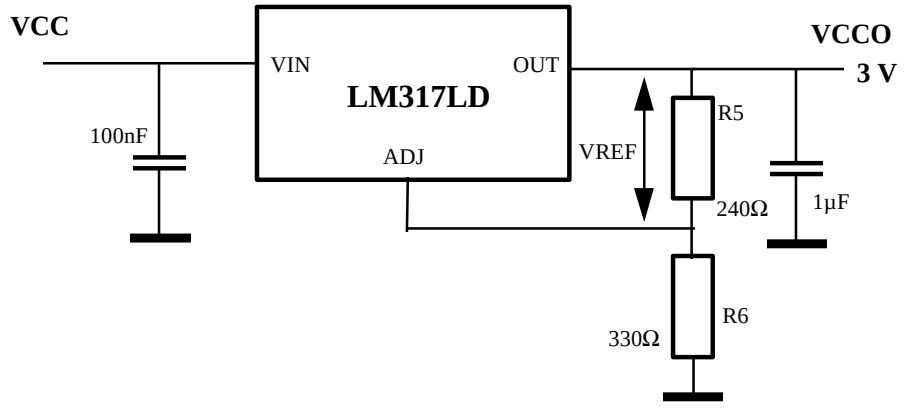
$$R4 = R3 \cdot \left(\frac{VCCD}{V_{REF}} - 1 \right) \qquad \text{thus,} \qquad R4 = 680\ W$$

A decoupling capacitor of 6.8µF connected between ADJ pin and Ground allows to improve the Supply Voltage Rejection of the regulator, *(SVR >65dB at F=120Hz)*. The input and output decoupling capacitors of respectively 100nF and 1µF were implanted close to the respective pin of the regulator. Taking into account all circuitry supplied with VCCD, the typical consumption ICCD is about 90 mA.

6.4 3V LOW VOLTAGE OUTPUT DIGITAL REGULATION - VCCO

The Demo-Board is designed to supply the compatible CMOS output buffer stages of the TDA8768 under VCCO = 3V *(corresponding to Low voltage Logic compatibility).*

In fact, the proposed diagram is shown on the **Figure 18**. The same principle as before *(VCCD regulation)* was used.



- FIGURE 18 -

In order to obtain a Low voltage value of VCCO the value of the resistor R5 must satisfy the following relation :

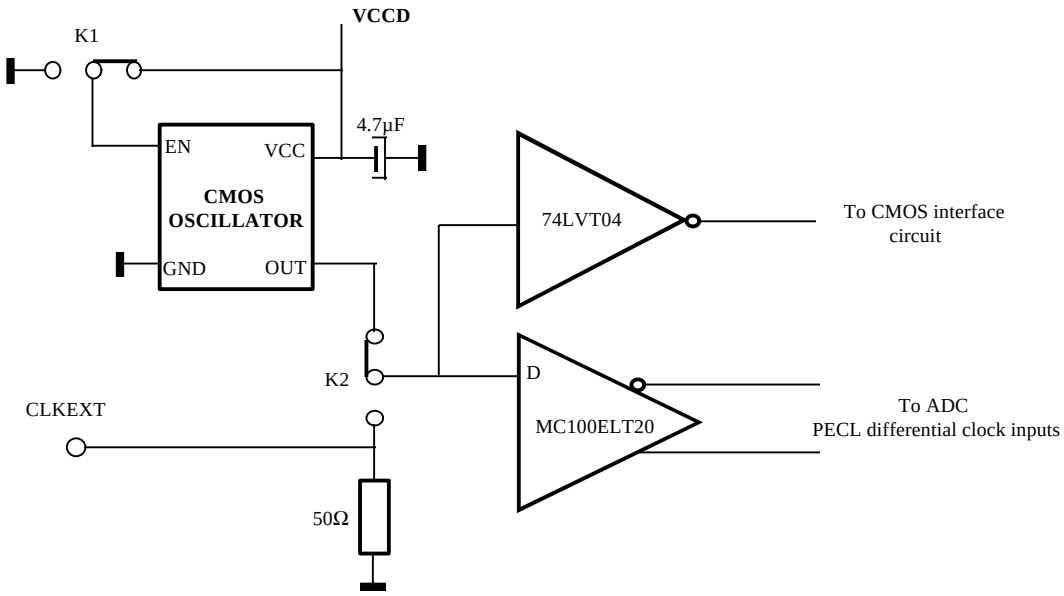
$$VCCO = V_{REF} \cdot \frac{R6 + R5}{R5}$$

with R5 = 240Ω fixed we obtain :

$$R6 = R5 \cdot \left(\frac{VCCO}{V_{REF}} - 1 \right) \qquad \text{thus,} \qquad R6 = 330\ W$$

6.5 ADC CLOCK GENERATION

A specific circuit has been designed to produce the internal clock signal available on the Demonstration-Board. The proposed circuit is shown in **Figure 19**.



- FIGURE 19 -

A three state CMOS compatible oscillator Hybrid circuit type ½ format of KONY was used to create the 40 or 50 MHz clock signal, available on the Demonstration-Board. The output clock signal is applied on the input of the CMOS Low voltage inverted Buffer type 74LVT04 *(used to ensure the clock synchronization on the output CMOS interface circuit)* and the input of the TTL to PECL translator IC *(used to produce the ADC differential clock signal)* through the switch selector K2. An chip Enable control *(active high)* of the oscillator is available on the demonstration-Board with switch K1.

Taking into account the frequency stability coefficient *(± 100 ppm)* of the TTL oscillator an evaluation of the short term jitter t_{jitt} can be made from the hereunder relation :

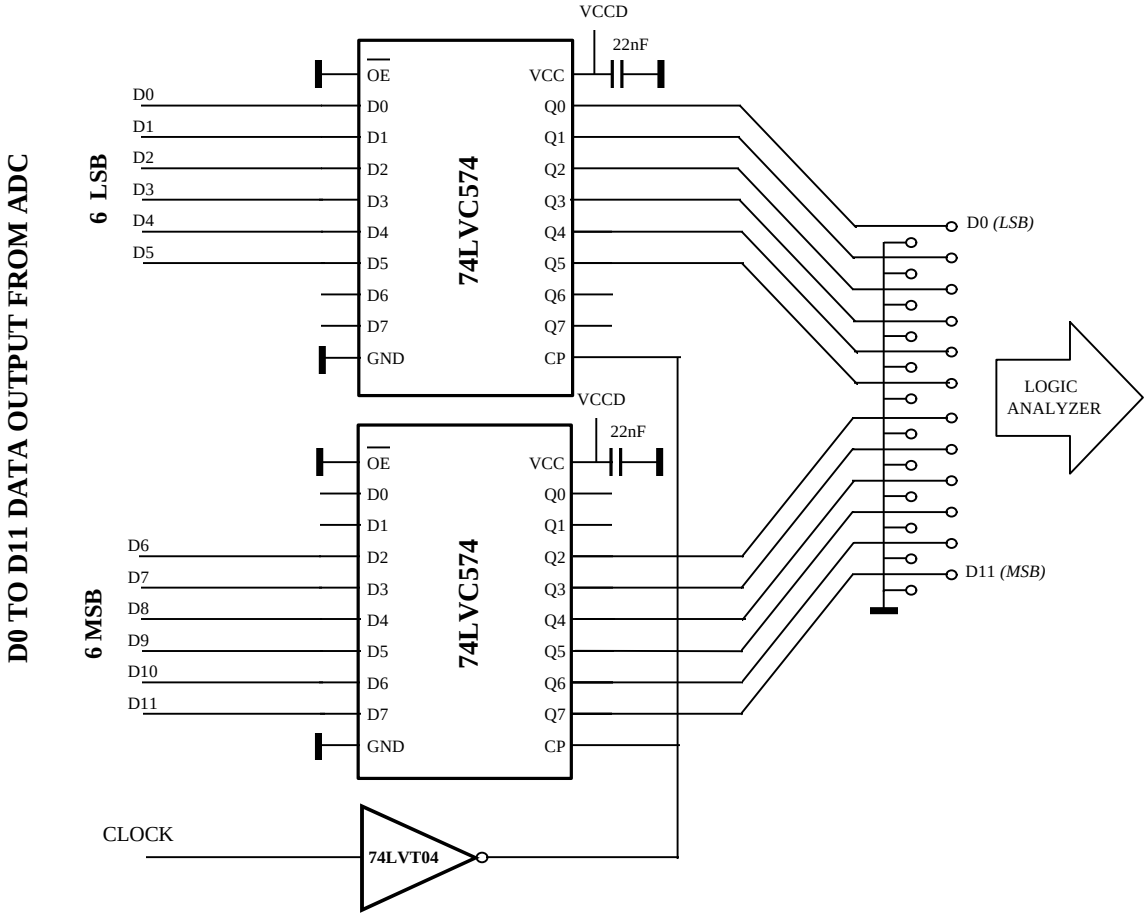
$$t_{jitt} = \frac{2DF}{F_0^2 - DF^2}$$

where ΔF is the maximum drift frequency and F_0 the fundamental frequency *(50MHz)* of the oscillator. After computation we obtain :

$$t_{jitt} = 4\ ps$$

6.6 CMOS-COMPATIBLE INTERFACE CIRCUIT

The electrical diagram of this circuit is shown on the **Figure 20**, it allows to recover the ADC data output synchronized on the clock falling sampling edge.



- FIGURE 20 -

This circuit uses two SMD ICs D Flip-Flop type 74LVC574 of the CMOS Low Voltage Logic Family in SSOP package. The recovered data output are directly addressed to the special probe test points, through the 50Ω microstrip lines. The main characteristics obtained on the recovered eye diagram D0 on the output D Flip-Flop, with a internal clock sampling of 50 MSps are the following:

High Level	*: VOH = 2.8 V*	*Rise time*	*: t_r =2.2 ns*
Low Level	*: VOL = 0.1 V*	*Fall time*	*: t_f =2.2 ns*

7. PERFORMANCES

An evaluation of the performances of the TDA8768H Analog to Digital Converter was made on the dynamic test bench, with Demonstration Board environment.

7.1 EXTERNAL SAMPLING CLOCK MODE

The main results obtained from the Fast Fourier Transformation *(FFT)* for different correlated frequencies of the Full Scale analog signal of 4.43 and 21.4MHz and the following conditions :

Antialiasing filters	:	Fa = 4.43 and 20 MHz
Sampling clock frequencies	:	Fclk = 50 and 60 MHz
Sample & Hold function	:	ON

are given in the herunder tables :

F_{in} = 4.43 MHz Full Scale SW

F_{clock} *(MHz)*	THD *(dB)* *(1)*	SINAD *(dB)* *(2)*	SNR *(db)* *(3)*	ENOB *(4)*
50.021	- 72.01	64.95	65.9	10.5
60.434	- 68.27	62.67	64.07	10.12

F_{in} = 21.4 MHz Full Scale SW

F_{clock} *(MHz)*	THD *(dB)* *(1)*	SINAD *(dB)* *(2)*	SNR *(db)* *(3)*	ENOB *(4)*
50	- 61.85	59.5	63.4	9.6

Note : In practice, in order to obtain a correlation between the clock and analog signals the analog frequencies are automatically adjusted *(near mentionned values)* on the measurement bench. This allows to limit the clock jitter effect on the reconstruction of the analog input signals with a number of aquisition points higher than N0 = 16 K.

7.2 INTERNAL CLOCK WITH S&H MODE

An acquisition was made with the 50 MHz internal clock signal, the main result obtained are given on the hereunder table :

F_{in} = 4.43 MHz Full Scale SW

F_{clock} *(MHz)*	THD *(dB)* *(1)*	SINAD *(dB)* *(2)*	SNR *(db)* *(3)*	ENOB *(4)*
50	- 71.77	64.3	65.2	10.4

Note : In the case where the internal clock signal is used, the analog frequency signal can not be automatically correlated with the clock frequency available on the Demo-Board, consequently in order to reduce the clock jitter effect with regard to analog signal, a number of acquisition points N0 must be limited to about some thousand points.

(1) - THD " Total Harmonics Distorsion" is obtained with the addition of the first five harmonics :

$$THD = 20\log F \Big/ \sqrt{(2nd)^2 + (3rd)^2 + (4th)^2 + (5th)^2 + (6th)^2}$$

(2) - SINAD " Signal to Noise And Distorsion ratio " taking into account all harmonics.

(3) - SNR " Signal to Noise Ratio " without all harmonics.

(4) - Effective Number of Bits are obtained from FFT. The computation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). The conversion to SINAD is given by :

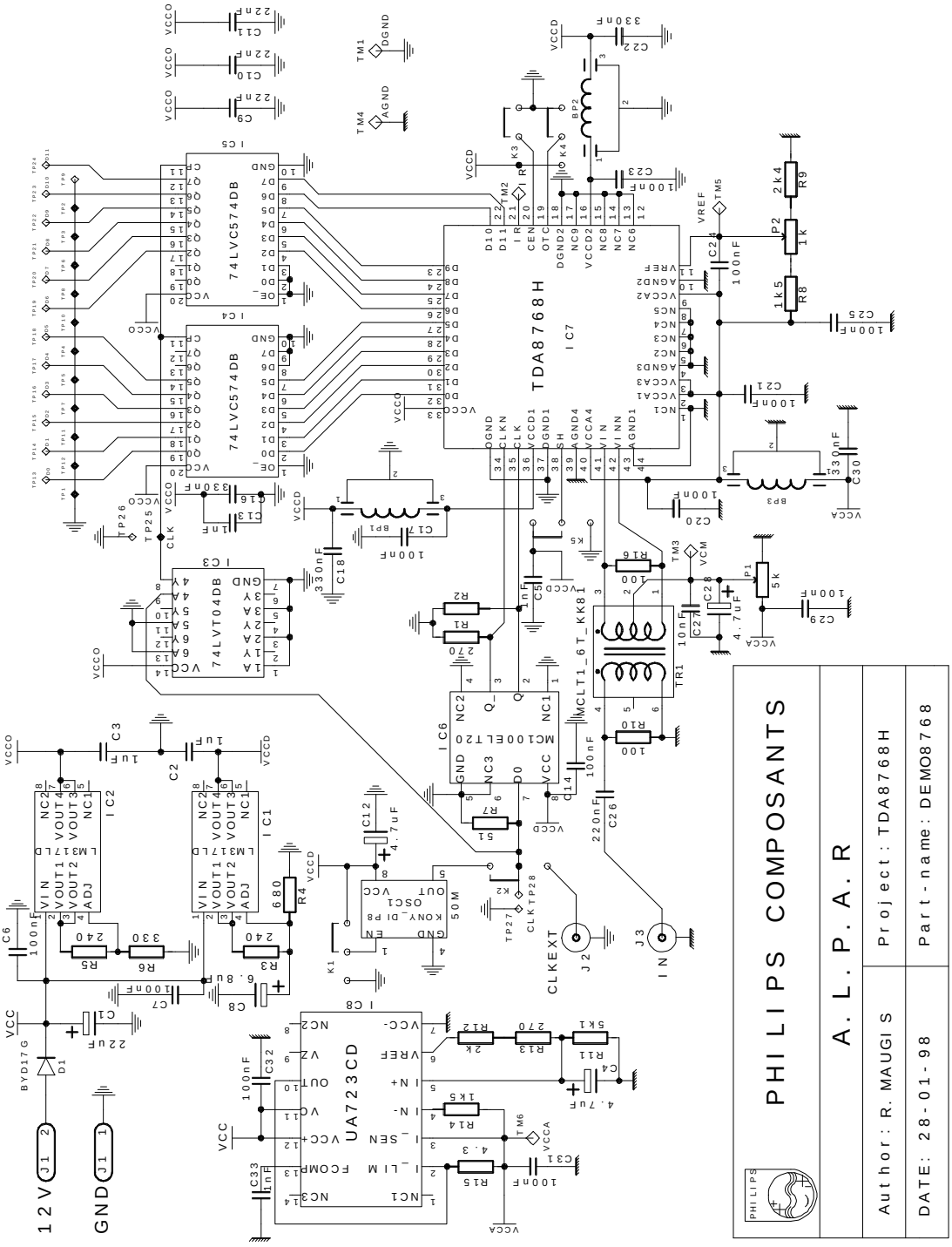
$$SINAD = ENOB \cdot 6.02 + 1.76dB$$

8. DEMO-BOARD FILE

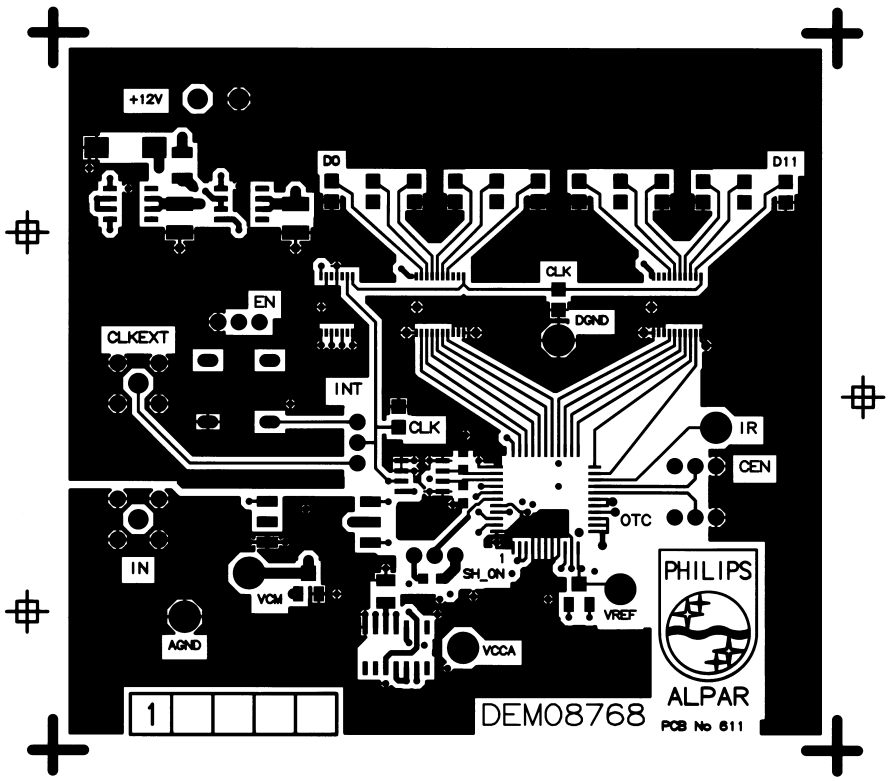
The following documents are shown in the **Figure 21 to 28**:

- Electrical diagram.
- Double sided layout.
- Internal ground planes.
- Internal layer supply layout.
- Double sided components implantation.

The part list with the values and references of all the components used is given in the **tables 1 to 3**.


PHILIPS COMPOSANTS
A.L.P.A.R
Author: R. MAUGIS
Project: TDA8768H
DATE: 28-01-98
Part-name: DEMO8768
TDA8768H
74LVC574DB
74LVT04DB
MC100ELT20
MCLT1_6T_KK81
LM317LD
UA723CD
12V
GND
CLKEXT

- FIGURE 21 -



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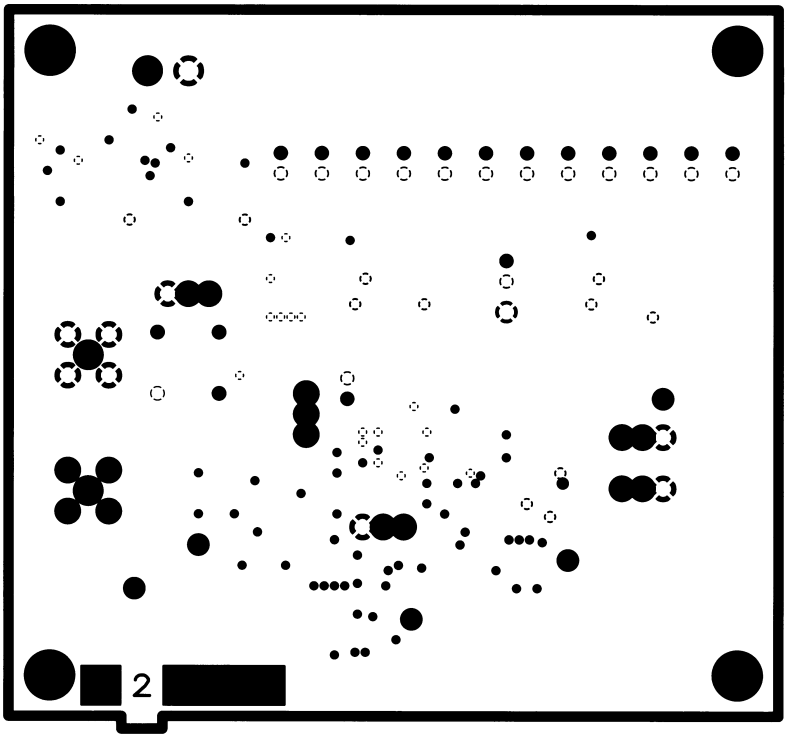
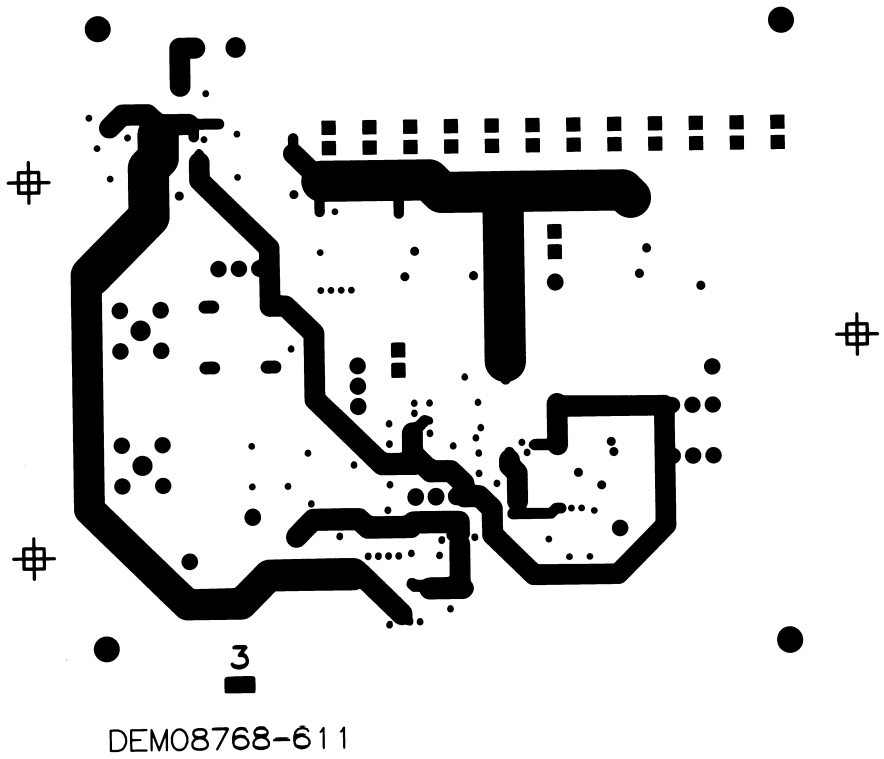
- FIGURE 22 -

OVERSIDE LAYOUT



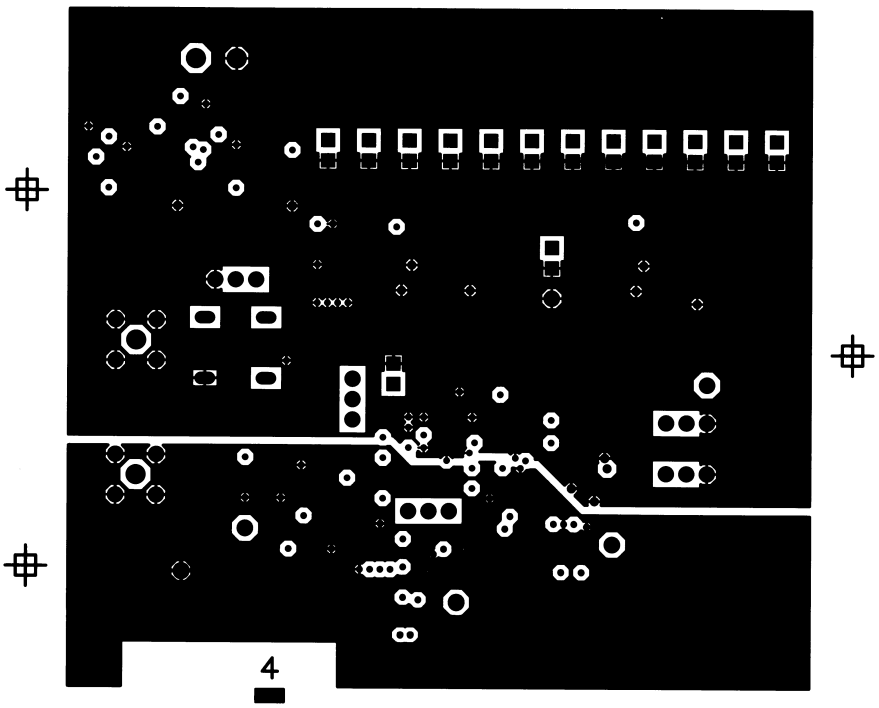
- FIGURE 23 -

INTERNAL GROUND PLANE - SECOND LAYER -



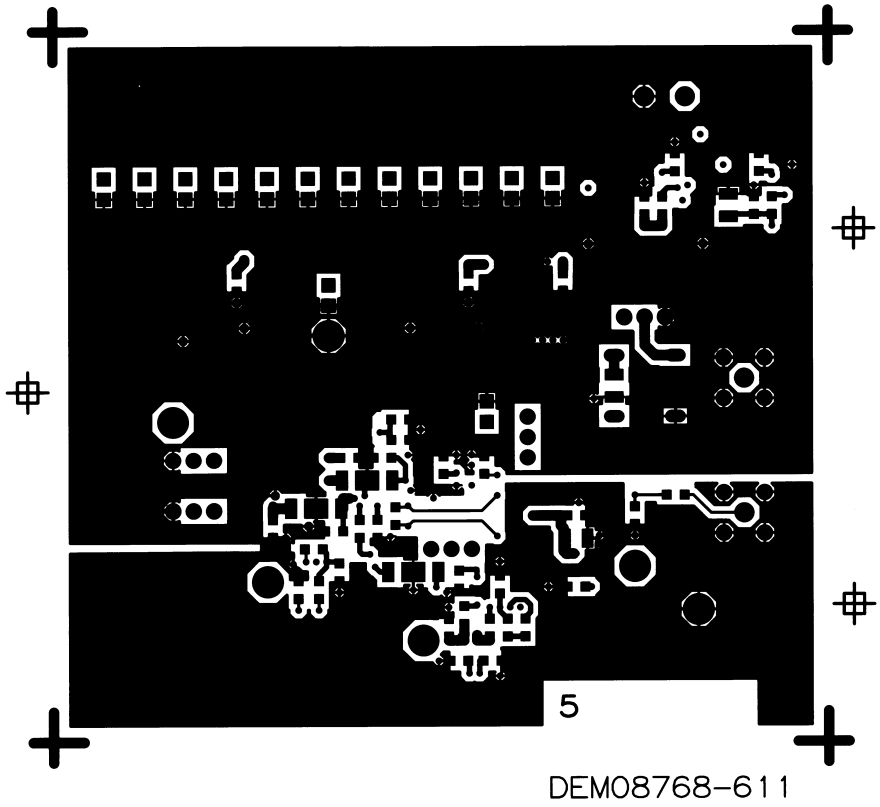
- FIGURE 24 -

INTERNAL SUPPLY PLANE - THIRD LAYER -



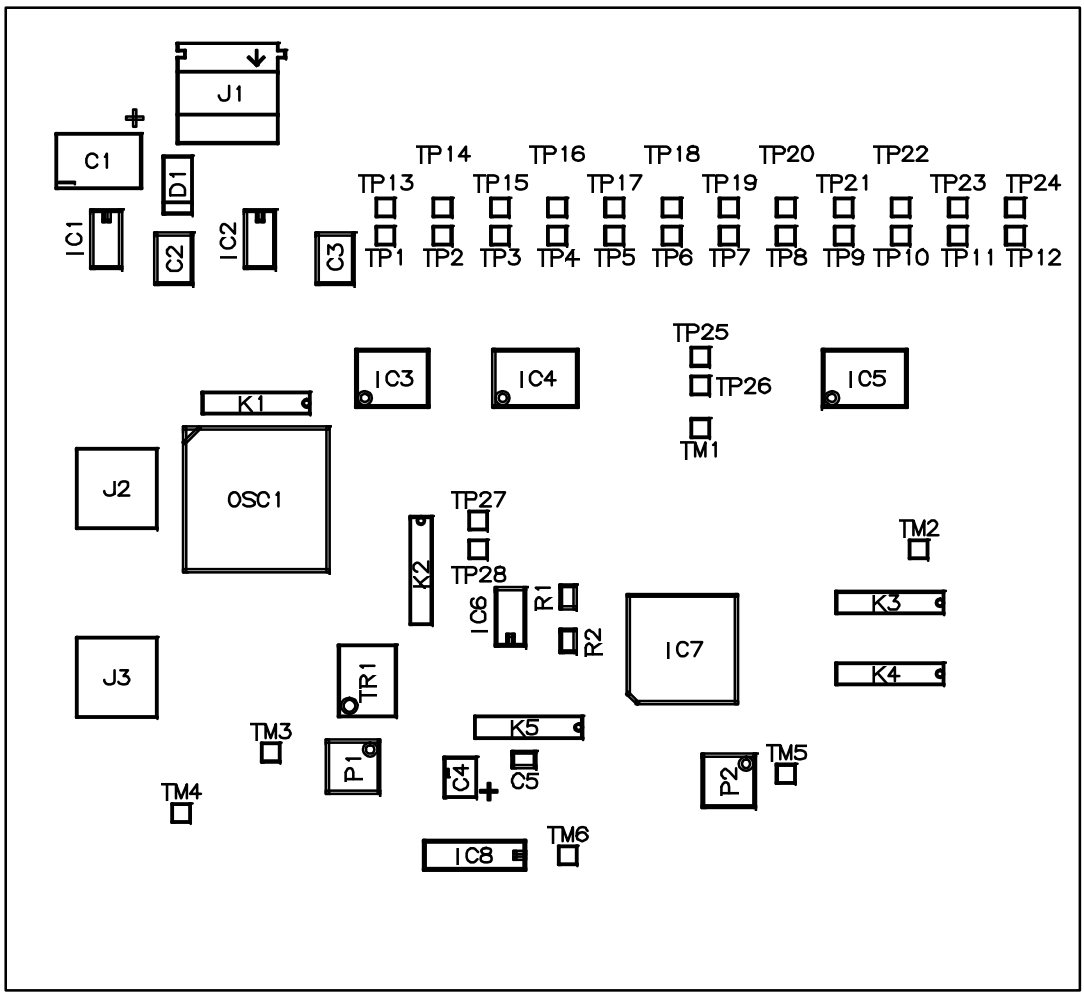
- FIGURE 25 -

INTERNAL DIGITAL AND ANALOG GROUND PLANES
- FOURTH LAYER -



- FIGURE 26 -

UNDERSIDE LAYOUT



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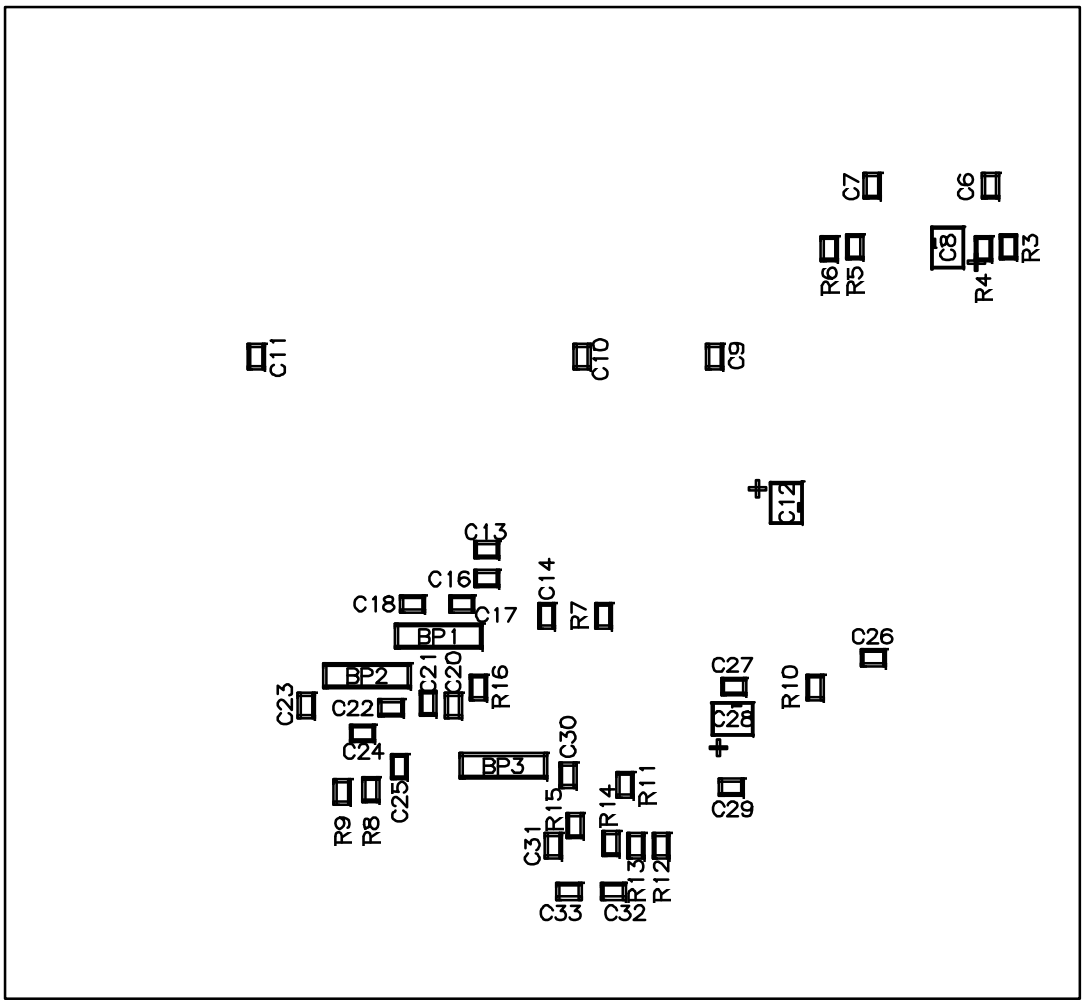
- FIGURE 27 -

OVERSIDE COMPONENTS IMPLANTATION



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- FIGURE 28 -

UNDERSIDE COMPONENTS IMPLANTATION

REFERENCES	VALUES	CODE NUMBER	MANUFACTURER
IC1	REGULATOR	LM317LD	SGS-THOMSON
IC2	-	-	-
IC3	INVERTER	74LVT04DB	PHILIPS
IC4	D FLIP-FLOP	74LVC574DBD	PHILIPS
IC5	-	-	-
IC6	TRANSLATOR	MC100ELT20	MOTOROLA
IC7	ADC	TDA8768H/5	PHILIPS
	-	TDA8768H/4	-
IC8	REGULATOR	µA723CD	PHILIPS
D1	SMD DIODE	BYD17G	PHILIPS
TR1	RF TRANSFORMER	MCLT1-6T - KK81	MINI CIRCUIT
OSC1	CMOS-OSCILLATOR	KTH089C 50MHz	KONY
	-	KTH089C 40MHz	-
BP1	PI FILTER 2nF	4700- 003-S	TUSONIX
BP2	-	-	-
BP3	-	-	-
J1	EDGE	MKSD 1.5/2-5.08	PHOENIX CONTACT
J2	50Ω-SMA	R125 426	RADIALL
J3	-	-	-
P1	POTENTIOMETER	3224 W 5k	BOURNS
P2	-	3224 W 1k	-
K1	SWITCH 1C/2P	09 03201 02	SECME
K2	-	-	-
K3	-	-	-
K4	-	-	-
K5	-	-	-

- TABLE 1 -

REFERENCES	VALUES	CODE NUMBER	MANUFACTURER
R1	SMD 270Ω	0805	PHILIPS
R2	-	-	-
R3	SMD 2400Ω	-	-
R4	SMD 680Ω	-	-
R5	SMD 240Ω	-	-
R6	SMD 330Ω	-	-
R7	SMD 51Ω	-	-
R8	SMD 1.5kΩ	-	-
R9	SMD 2.4kΩ	-	-
R10	SMD 100Ω	-	-
R11	SMD 5.1kΩ	-	-
R12	SMD 2 kΩ	-	-
R13	SMD 270Ω	-	-
R14	SMD 1.5 kΩ	-	-
R15	SMD 4.3Ω	-	-
R16	SMD 100Ω	-	-
C1	22µF/16V	293D226X9016D	SPRAGUE
C4	4.7µF/10V	293D475X9010B	SPRAGUE
C12	-	-	-
C28	-	-	-
C8	6.8µF/6V3	293D685X96R3B	SPRAGUE
C2	SMD 1µF	C1812	PHILIPS
C3	-	-	-
C16	SMD 330 nF	C0805	PHILIPS
C18	-	-	-
C22	-	-	-
C30	-	-	-
C26	SMD 220 nF	C0805	PHILIPS

- TABLE 2 -

REFERENCES	VALUES	CODE NUMBER	MANUFACTURER
C6	SMD 100nF	C0805	PHILIPS
C7	-	-	-
C14	-	-	-
C17	-	-	-
C20	-	-	-
C21	-	-	-
C23	-	-	-
C24	-	-	-
C25	-	-	-
C29	-	-	-
C31	-	-	-
C32	-	-	-
C9	SMD 22nF	C0805	PHILIPS
C10	-	-	-
C11	-	-	-
C27	SMD 10nF	C0805	PHILIPS
C5	SMD 1 nF	C0805	PHILIPS
C33	-	-	-
TM1	BOLT HOLD	3110415000530	COMATEL
TM2	-	-	-
TM3	-	-	-
TM4	-	-	-
TM5	-	-	-
TM6	-	-	-
TP25/26	TEST POINT	3850358102400	COMATEL
TP27/28	-	-	-
TP1 to TP24	TEST PROBE	12X TEST POINTS	-

- TABLE 3 -